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		Application Number	10/761,613		
		Filing Date	1-21-04		
		First Named Inventor	chui		
		Art Unit	2823		
		Examiner Name	J. Garcia		
Sheet	2	of	2	Attorney Docket Number	cs03-050

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JAK		Inaba, et al., "silicon on depletion layer FET (SODEL FET) for sub - 50 nm high performance... by selective Si epi growth technology," 2002, IEEE	

Examiner Signature	<i>J. Garcia</i>	Date Considered	<i>March 8, 2005</i>
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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